VLSI Lab Assignment-2 Report

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**Aim and Objective of the Lab:**

To write Verilog codes for MUX, DEMUX, ENCODER & DECODER and to compare power, fabrication area, etc. Also, to complete the flow for dumping code on the FPGA.

**Introduction:**

In this lab assignment, we have used tools such as **Xilinx ISE** *(to write and test Verilog codes and to generate .bit files for programming FPGA)*, **Genus** *(to generate area, power and timing reports)* and **Innovus** *(to optimise the fabrication area and power of the circuit)*.

We also compared the fabrication area and power of different circuits, and dumped our codes on Nexys2 FPGA.

**Procedure:**

1. We wrote the codes and testbench files for different combination logic circuits in Verilog.
2. We generated the timing diagrams and RTL Schematics for the codes using Xilinx ISE.
3. We also generated timing diagrams using NCLaunch.
4. We generated power and area reports using Genus.
5. We optimized the power and fabrication area using Innovus.
6. We dumped code on Nexys2 using Digilent Adept.

**Results and Discussion:**

POWER OUTPUTS:

**>Genus:**

**MUX:**

**Leakage Dynamic Total**

**Instance Cells Power(nW) Power(nW) Power(nW)**

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**mux8x1** 7 379.277 1382.749 1762.027

Mux4x1\_1 3 162.547 474.841 637.388

Mux2x1\_1 1 54.182 148.907 203.089

Mux2x1\_2 1 54.182 119.868 174.051

Mux2x1\_3 1 54.182 206.066 260.248

Mux4x1\_2 3 162.547 416.813 579.360

Mux2x1\_1 1 54.182 148.907 203.089

Mux2x1\_2 1 54.182 119.868 174.051

Mux2x1\_3 1 54.182 148.038 202.220

Mux4x1\_3 1 54.182 154.439 208.622

Mux2x1\_1 1 54.182 154.439 208.622

**DEMUX:**

**Leakage Dynamic Total**

**Instance Cells Power(nW) Power(nW) Power(nW)**

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**demux1x8** 14 296.538 1274.541 1571.079

Demux1x4\_2 6 126.371 378.731 505.102

Demux1x2\_1 2 43.796 202.075 245.871

Demux1x2\_2 2 41.288 89.682 130.970

Demux1x2\_3 2 41.288 86.974 128.261

Demux1x4\_3 6 126.371 376.099 502.470

Demux1x2\_1 2 43.796 204.524 248.319

Demux1x2\_2 2 41.288 105.875 147.163

Demux1x2\_3 2 41.288 65.700 106.987

Demux1x4\_1 2 43.796 284.306 328.101

Demux1x2\_2 2 43.796 284.306 328.101

**ENCODER:**

**Leakage Dynamic Total**

**Instance Cells Power(nW) Power(nW) Power(nW)**

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**encoder8x3** 9 85.097 773.840 858.937

**DECODER:**

**Leakage Dynamic Total**

**Instance Cells Power(nW) Power(nW) Power(nW)**

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**decoder3x8**  14 296.538 1274.541 1571.079

Decoder2x4\_2 6 126.371 378.731 505.102

Decoder1x2\_1 2 43.796 202.075 245.871

Decoder1x2\_2 2 41.288 89.682 130.970

Decoder1x2\_3 2 41.288 86.974 128.261

Decoder2x4\_3 6 126.371 376.099 502.470

Decoder1x2\_1 2 43.796 204.524 248.319

Decoder1x2\_2 2 41.288 105.875 147.163

Decoder1x2\_3 2 41.288 65.700 106.987

Decoder2x4\_1 2 43.796 284.306 328.101

Decoder1x2\_2 2 43.796 284.306 328.101

**>Innovus:**

**MUX:**

Total Internal Power: 0.00099762 64.0033%

Total Switching Power: 0.00018181 11.6639%

Total Leakage Power: 0.00037928 24.3328%

Total Power: 0.00155871

**DEMUX:**

Total Internal Power: 0.00069752 57.5524%

Total Switching Power: 0.00021792 17.9804%

Total Leakage Power: 0.00029654 24.4672%

Total Power: 0.00121198

**ENCODER:**

Total Internal Power: 0.00045891 57.8297%

Total Switching Power: 0.00024955 31.4469%

Total Leakage Power: 0.00008510 10.7234%

Total Power: 0.00079356

**DECODER:**

Total Internal Power: 0.00069752 57.5524%

Total Switching Power: 0.00021792 17.9804%

Total Leakage Power: 0.00029654 24.4672%

Total Power: 0.00121198

AREA OUTPUTS:

**>Genus:**

**MUX:**

**Gate Instances Area Library**

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MX2X1 7 47.685 slow

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total 7 47.685

**Type Instances Area Area%**

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logic 7 47.685 100.0

physical\_cells 0 0.000 0.0

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total 7 47.685 100.0

**DEMUX:**

**Gate Instances Area Library**

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AND2X1 3 13.624 slow

AND2XL 4 18.166 slow

NOR2BXL 7 31.790 slow

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total 14 63.580

**Type Instances Area Area%**

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logic 14 63.580 100.0

physical\_cells 0 0.000 0.0

---------------------------------------

total 14 63.580 100.0

**ENCODER:**

**Gate Instances Area Library**

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AOI21XL 1 4.541 slow

INVXL 1 2.271 slow

NAND2XL 4 12.110 slow

OAI21XL 2 9.083 slow

OAI31XL 1 6.055 slow

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total 9 34.060

**Type Instances Area Area%**

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inverter 1 2.271 6.7

logic 8 31.790 93.3

physical\_cells 0 0.000 0.0

---------------------------------------

total 9 34.061 100.0

**DECODER:**

**Gate Instances Area Library**

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AND2X1 3 13.624 slow

AND2XL 4 18.166 slow

NOR2BXL 7 31.790 slow

-----------------------------------

total 14 63.580

**Type Instances Area Area%**

---------------------------------------

logic 14 63.580 100.0

physical\_cells 0 0.000 0.0

---------------------------------------

total 14 63.580 100.0

**>Innovus:**

**MUX:**

Depth Name #Inst Area (um^2)

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0 mux8x1 7 47.6847

1 Mux4x1\_3 1 6.8121

1 Mux4x1\_2 3 20.4363

1 Mux4x1\_1 3 20.4363

2 Mux4x1\_2/Mux2x1\_3 1 6.8121

2 Mux4x1\_2/Mux2x1\_1 1 6.8121

2 Mux4x1\_1/Mux2x1\_3 1 6.8121

2 Mux4x1\_1/Mux2x1\_1 1 6.8121

2 Mux4x1\_3/Mux2x1\_1 1 6.8121

2 Mux4x1\_2/Mux2x1\_2 1 6.8121

2 Mux4x1\_1/Mux2x1\_2 1 6.8121

**DEMUX:**

Depth Name #Inst Area (um^2)

--------------------------------------------------

0 demux1x8 14 63.5796

1 Demux1x4\_3 6 27.2484

1 Demux1x4\_2 6 27.2484

1 Demux1x4\_1 2 9.0828

2 Demux1x4\_3/Demux1x2\_1 2 9.0828

2 Demux1x4\_2/Demux1x2\_3 2 9.0828

2 Demux1x4\_2/Demux1x2\_1 2 9.0828

2 Demux1x4\_1/Demux1x2\_2 2 9.0828

2 Demux1x4\_3/Demux1x2\_3 2 9.0828

2 Demux1x4\_3/Demux1x2\_2 2 9.0828

2 Demux1x4\_2/Demux1x2\_2 2 9.0828

**ENCODER:**

Depth Name #Inst Area (um^2)

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0 encoder8x3 9 34.0605

**DECODER:**

Depth Name #Inst Area (um^2)

------------------------------------------------------

0 decoder3x8 14 63.5796

1 Decoder2x4\_3 6 27.2484

1 Decoder2x4\_2 6 27.2484

1 Decoder2x4\_1 2 9.0828

2 Decoder2x4\_3/Decoder1x2\_1 2 9.0828

2 Decoder2x4\_2/Decoder1x2\_3 2 9.0828

2 Decoder2x4\_2/Decoder1x2\_1 2 9.0828

2 Decoder2x4\_1/Decoder1x2\_2 2 9.0828

2 Decoder2x4\_3/Decoder1x2\_3 2 9.0828

2 Decoder2x4\_3/Decoder1x2\_2 2 9.0828

2 Decoder2x4\_2/Decoder1x2\_2 2 9.0828

**Conclusion:**

Thus, from the observations we can conclude that with increase in the number of gates, the fabrication area and power increases.

Also, we see that after optimization, most of the times the area and power get reduced.

**Refernces:**

* Links provided on News forum: https://drive.google.com/open?id=1DkpjyA1jlUY42pv-zL3H0AUn\_PxH4NKe